CLAIMS

We claim:

1. A signal synthesizer (e.g., **208**) comprising a loop filter (e.g., **214**) connected between a charge pump (e.g., **212**) and an oscillator (e.g., **216**) of the signal synthesizer to accumulate charge from the charge pump and generate at least a first control signal (e.g., V_{CTRL}) for the oscillator, the loop filter comprising:

a damping capacitor (e.g., C1) connected at a first node to a resistor (e.g., R1) to generate the first control signal for the oscillator;

a matching capacitor (e.g., C1'); and

sensing-and-canceling circuitry (e.g., **502, 504, 506**) adapted to (1) drive a voltage across the matching capacitor to match a first reference voltage (e.g., V_{REF}) and (2) generate, based on a first current associated with driving the voltage across the matching capacitor, a second current applied to the damping capacitor to compensate for leakage current in the damping capacitor.

2. The invention of claim 1, wherein:

the signal synthesizer is a PLL;

a first side of the resistor is connected to the damping capacitor;

a second side of the resistor is connected to both the charge pump and the oscillator; and

the first control signal is generated based on a voltage at the second side of the resistor.

3. The invention of claim 1, wherein the oscillator is adapted to use the first control signal for steady-state control of the synthesizer.

4. The invention of claim 1, wherein the sensing-and-canceling circuitry comprises:

an operational amplifier (op amp) (e.g., **502**) adapted to generate a voltage difference signal based on a difference between the voltage across the matching capacitor and the first reference voltage;

a first transistor (e.g., **504**) connected (1) to receive the voltage difference signal from the op amp at a gate of the first transistor and (2) to apply a first transistor output signal to the matching capacitor; and

a second transistor (e.g., **506**) connected (1) to receive the voltage difference signal from the op amp at a gate of the second transistor and (2) to apply a second transistor output signal to the damping capacitor.

5. The invention of claim 1, wherein gate oxide thickness of the damping capacitor is substantially less than about 50 Angstroms.

6. The invention of claim 5, wherein the gate oxide thickness of the damping capacitor is about 17 Angstroms or less.

7. The invention of claim 1, wherein the sensing-and-canceling circuitry is adapted to generate the second current as a scaled version of the first current based on a capacitance ratio between the damping capacitor and the matching capacitor.

8. The invention of claim 1, wherein the loop filter further comprises a transconductor capacitor (e.g., C3) connected to generate a second control signal (e.g., V_{BG}) for the oscillator.

9. The invention of claim 8, wherein gate oxide thickness of the transconductor capacitor is substantially less than about 50 Angstroms.

10. The invention of claim 9, wherein the gate oxide thickness of the transconductor capacitor is about 17 Angstroms or less.

11. The invention of claim 8, wherein the oscillator is adapted to use the second control signal to set a center frequency for the oscillator.

12. The invention of claim 8, wherein the loop filter further comprises an analog transconductor (gm) cell connected between (1) the first node and (2) the transconductor capacitor, wherein the gm cell is adapted to generate a first gm output signal based on a difference between a voltage at the first node and a second reference voltage (e.g., V_{REF}), wherein the first gm output signal is applied to the transconductor capacitor.

13. The invention of claim 12, wherein the second reference voltage is equal to the first reference voltage.

14. The invention of claim 12, wherein the loop filter further comprises a digital gm path (e.g., **702, 704, 706**) adapted to (1) digitally accumulate differences between the voltage at the first node and the second reference voltage and (2) generate a second gm output signal based on the accumulated differences, wherein the second gm output signal is also applied to the transconductor capacitor.

15. The invention of claim 14, wherein the digital gm path comprises:

a comparator (e.g., **702**) adapted to generate digital differences between the voltage at the first node and the second reference voltage;

an accumulator (e.g., **704**) adapted to accumulate the digital differences; and

a converter (e.g., **706**) adapted to convert the accumulated digital differences from the accumulator into the second gm output signal.

16. The invention of claim 8, wherein the loop filter further comprises a digital gm path (e.g., **602**, **604**, **606**) adapted to (1) digitally accumulate differences between the voltage at the first node and the second reference voltage and (2) generate a gm output signal based on the accumulated differences, wherein the gm output signal is applied to the transconductor capacitor.

17. The invention of claim 16, wherein the digital gm path comprises:

a comparator (e.g., **602**) adapted to generate digital differences between the voltage at the first node and the second reference voltage;

an accumulator (e.g., **604**) adapted to accumulate the digital differences; and

a converter (e.g., **606**) adapted to convert the accumulated digital differences from the accumulator into the gm output signal.

18. The invention of claim 16, wherein the converter is a voltage source adapted to generate the gm output signal as a voltage signal.

19. The invention of claim 16, wherein the converter is a current source adapted to generate the gm output signal as a current signal.

20. A signal synthesizer (e.g., **208**) comprising a loop filter (e.g., **214**) connected between a charge pump (e.g., **212**) and an oscillator (e.g., **216**) of the signal synthesizer to accumulate charge from the charge pump and generate at least a first control signal (e.g., V_{BG}) for the oscillator, the loop filter comprising:

a resistor (e.g., R1);

a damping capacitor (e.g., C1) connected at a first node to the resistor;

a transconductor capacitor (e.g., C3) connected to generate the first control signal for the oscillator; and

a digital gm path (e.g., **602-606** or **702-706**) adapted to (1) digitally accumulate differences between a reference voltage (e.g., V_{REF}) and a voltage at the first node and (2) generate a first gm output signal

based on the accumulated differences, wherein the first gm output signal is applied to the transconductor capacitor.

21. The invention of claim 20, wherein the signal synthesizer is a PLL.

22. The invention of claim 20, wherein gate oxide thickness of the transconductor capacitor is substantially less than about 50 Angstroms.

23. The invention of claim 22, wherein the gate oxide thickness of the transconductor capacitor is about 17 Angstroms or less.

24. The invention of claim 20, wherein the oscillator is adapted to use the first control signal to set a center frequency for the oscillator.

25. The invention of claim 20, wherein the loop filter further comprises an analog transconductor (gm) cell (e.g., Gm of Fig. 7) connected between (1) the first node and (2) the transconductor capacitor, wherein the gm cell is adapted to generate a second gm output signal based on a difference between the voltage at the first node and the reference voltage, wherein the second gm output signal is also applied to the transconductor capacitor.

26. The invention of claim 20, wherein the digital gm path comprises:

a comparator (e.g., **602** or **702**) adapted to generate digital differences between the voltage at the first node and the reference voltage;

an accumulator (e.g., **604** or **704**) adapted to accumulate the digital differences; and

a converter (e.g., **606** or **706**) adapted to convert the accumulated digital differences from the accumulator into the second gm output signal.

27. The invention of claim 26, wherein the converter is a voltage source adapted to generate the second gm output signal as a voltage signal.

28. The invention of claim 26, wherein the converter is a current source adapted to generate the second gm output signal as a current signal.

29. A signal synthesizer (e.g., **208**) comprising a loop filter (e.g., **214**) connected between a charge pump (e.g., **212**) and an oscillator (e.g., **216**) of the signal synthesizer to accumulate charge from the charge pump and generate at least a first control signal (e.g., V_{CTRL} or V_{BG}) for the oscillator, the loop filter comprising:

a capacitor (e.g., C1 or C3) connected to contribute to the generation of the first control signal for the oscillator; and

sensing-and-canceling circuitry (e.g., C1' and **502-506** of Fig. 5 or **602-606** of Fig. 6 or **702-706** of Fig. 7) adapted to generate a current applied to the capacitor to compensate for leakage current in the capacitor.

30. The invention of claim 29, wherein:

the capacitor is a damping capacitor (e.g., C1) connected to a resistor (e.g., R1) to generate the first control signal (e.g., V_{CTRL}) for the oscillator; and

the sensing-and-canceling circuitry comprises a matching capacitor (e.g., C1'), wherein the sensing-and-canceling circuitry is adapted to (1) drive a voltage across the matching capacitor to match a first reference voltage (e.g., V_{REF}) and (2) generate, based on a first current associated with driving the voltage across the matching capacitor, a second current applied to the damping capacitor to compensate for leakage current in the damping capacitor.

31. The invention of claim 29, wherein:

the capacitor is a transconductor capacitor (e.g., C3) connected to generate the first control signal (e.g., V_{BG}) for the oscillator; and

the loop filter further comprises a digital gm path (e.g., **602-606** or **702-706**) adapted to (1) digitally accumulate differences between (i) a voltage at a first node in the loop filter and (ii) a first reference voltage (e.g., V_{REF}) and (2) generate a first gm output signal based on the accumulated differences, wherein the first gm output signal is applied to the transconductor capacitor to compensate for leakage current in the capacitor.

32. The invention of claim 31, wherein the loop filter further comprises an analog transconductor (gm) cell (e.g., Gm of Fig. 7) connected between (1) the first node and (2) the transconductor capacitor, wherein the gm cell is adapted to generate a second gm output signal based on a difference between the voltage at the first node and the first reference voltage, wherein the second gm output signal is also applied to the transconductor capacitor.

33. The invention of claim 29, wherein gate oxide thickness of the capacitor is substantially less than about 50 Angstroms.

34. The invention of claim 33, wherein the gate oxide thickness of the capacitor is about 17 Angstroms or less.